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182-000

PART NUMBER
R6500/1E

Rockwell

R6500 Microcomputer System DATA SHEET SUPPLEMENT

R6500/1E EMULATOR DEVICE

INTRODUCTION

To aid in designing R6500/1 microcomputer systems, Rockwell has developed a PROM compatible, 64-pin, R6500/1E Emulator device. The architecture of the Emulator device is basically the same as the R6500/1 except that the address, data, and associated control lines are routed off the chip for connection to an external memory.

The functions and operation of the Emulator device are identical to the R6500/1 with only some minor differences, described herein. The R6500/1 data sheet (Document No. 2900D51) contains the description of R6500/1 and R6500/1 common interface signals and functions.

ORDERING INFORMATION

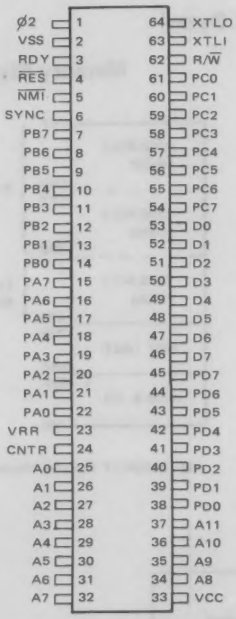
Order Number	Package Type	Frequency Option	Temperature Range
R6500/1EC	Ceramic	1 MHz	0°C to 70°C
R6500/1EAC	Ceramic	2 MHz	0°C to 70°C

SIGNAL DESCRIPTIONS

All R6500/1 interface signals are provided in the Emulator device. While the Emulator pin assignments are different from the R6500/1 in order to accommodate the 64-pin Emulator package, the interface electrical characteristics are identical. The Emulator device provides 24 additional signals to route the address bus (12 lines), the data bus (8 lines), and control signals (4 lines) off the chip for connection to external memory.

MEMORY MAP

An additional 1024 bytes of memory (400-7FF) are addressable in the Emulator device to support software development.



R6500/1E Pin Configuration

EXTERNAL FREQUENCY REFERENCE

The external frequency reference may be a crystal or a clock — the RC option is not available in the Emulator device.

I/O PORT PULLUPS

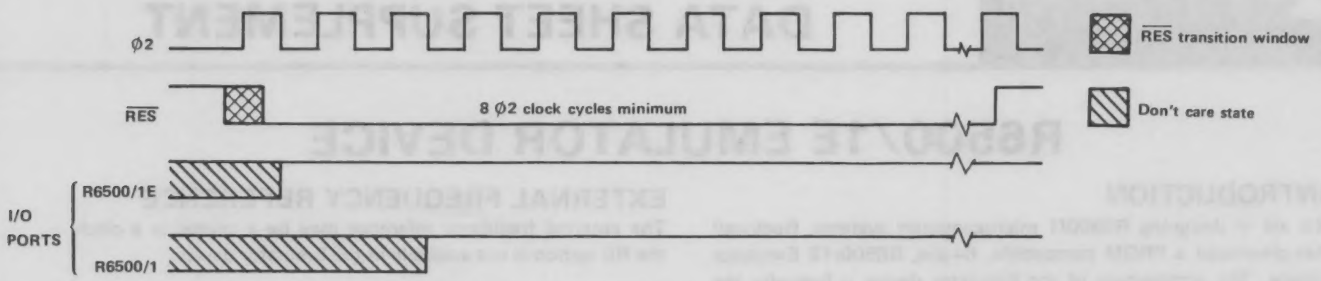
The R6500/1E has the internal I/O port pullup resistance only.

R6500/1E DEVICE ADDITIONAL SIGNALS

Signal Name	Pin No.	Description
R/$\overline{W}$	62	Read/Write. The Read/Write output controls the direction of data transfer between the R6500/1E Emulator CPU and external memory. This line is high when reading data from memory and low when writing data to memory.
RDY	3	Ready. The Ready input delays execution of any cycle during which the RDY line is low. This allows the user to halt or single step the CPU on any cycle except a write cycle. A negative transition to the low state during the φ2 clock low pulse will halt the CPU with the address lines containing the current address being fetched. If RDY is low during a write cycle, it is ignored until the following read operation. This condition will remain through a subsequent φ2 clock pulse in which the RDY line is low.
SYNC	6	Sync. The Sync signal is provided to identify those cycles in which the CPU is performing an OP CODE fetch. SYNC goes high during φ2 clock-low pulse during an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the φ2 clock low pulse in which SYNC went high, the CPU will halt in its current state and will remain in that state until the RDY line goes high. Using this technique, the SYNC signal can be used to control RDY to cause single instruction execution.
φ2	1	Phase 2 (φ2) clock pulse. Data transfer can take place only during φ2 clock pulse.
A0-A11	25-32 34-37	Address Bus Lines. The address bus buffers on the R6500/1E are push/pull type drivers capable of driving at least 130 pf and one standard TTL load. The address bus always contains known data. The addressing technique involves putting an address on the address bus which is known to be either in program sequence, on the same page in program memory, or at a known point in memory. The I/O addresses are also placed on these lines.
D0-D7	53-46	Data Bus Lines. All transfers of instructions and data between the CPU and external memory take place on the data bus lines. The buffers driving the data bus lines have full three-state capability. Each data bus pin is connected to an input and an output buffer, with the output buffer remaining in the floating condition.

R6500/1E I/O PORT INITIALIZATION

Ports A, B, C and D and the CNTR line in R6500/1E are initialized to the logic high state two Ø2 clock cycles earlier than in the R6500/1. It is still required, however, that the $\overline{RES}$ line to the R6500/1E be held low for at least eight Ø2 clock cycles after V_{CC} reaches operating range.



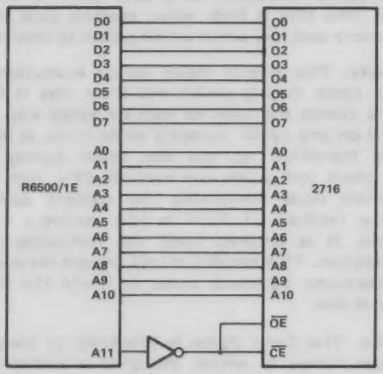
TYPICAL R6500/1E PROGRAM MEMORY INTERCONNECTIONS

Shown below are two typical connections between the R6500/1E and program memory (in this case, type 2716 and 2708 PROMS). Example 1 shows a connection to a 2K 2716 PROM. Since the R6500/1 has a 2K ROM capacity, the contents of the PROM could be masked directly into the production R6500/1 ROM.

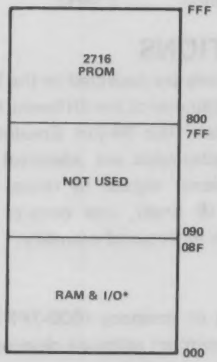
Example 2 shows a connection to 3K of 2708 PROMS. The extra 1K PROM allows expanded or additional programs be used during R6500/1 firmware development. The production program, however, must be reduced to 2K maximum (between addresses 800 and FFF) before committing to R6500/1 ROM.

EXAMPLE 1: R6500/1E Connected to One 2716 PROM (2K Bytes)

Connection Diagram

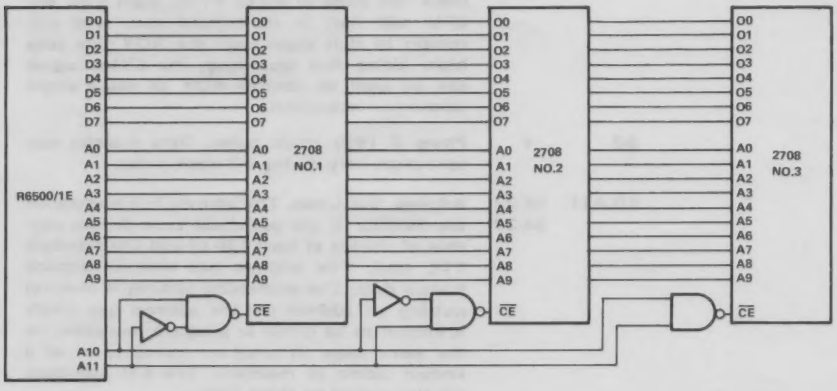


Memory Map

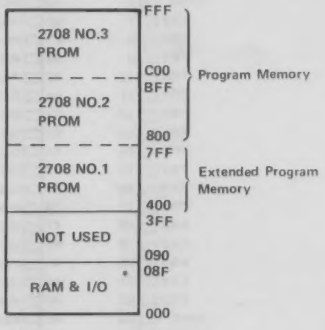


EXAMPLE 2: R6500/1E Connected to Three PROMS (3K Bytes)

Connection Diagram



Memory Map



*See R6500/1E Detailed Memory Map

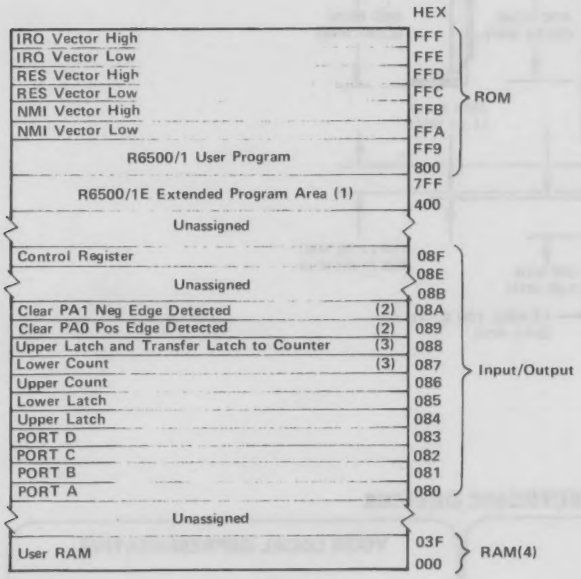
Truth Table

Address		PROM Select			
A11	A10	2708 No. 3 $\overline{CE}$	2708 No. 2 $\overline{CE}$	2808 No. 1 $\overline{CE}$	Selected Address Range
0	0	1	1	1	000-3FF
0	1	1	1	0	400-7FF
1	0	1	0	1	800-BFF
1	1	0	1	1	C00-FFF

R6500/1 EMULATOR DEVICE TIMING

Signal	Symbol	1 MHz		2 MHz		Unit
		Min.	Max.	Min.	Max.	
R/$\overline{W}$ setup time from CPU	T_{RWS}		300		200	ns
Address setup time from CPU	T_{ADS}		300		200	ns
Memory read access time	T_{ACC}		525		225	ns
Data stabilization time	T_{DSU}	150		75		ns
Data hold time — Read	T_{HR}	10		10		ns
Data hold time — Write	T_{HW}	30		30		ns
Data delay time from CPU	T_{MDS}		200		150	ns
RDY setup time	T_{RDY}	100		50		ns
SYNC delay time from CPU	T_{SYNC}		350		175	ns
Address hold time	T_{HA}	30		30		ns
R/$\overline{W}$ hold time	T_{HRW}	30		30		ns
Cycle Time	T_{CYC}	1.0	10.0	0.5	10.0	μs

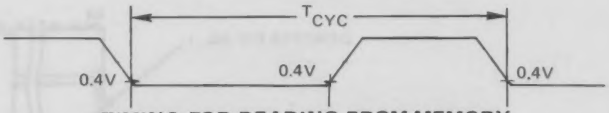
R6500/1E DETAILED MEMORY MAP



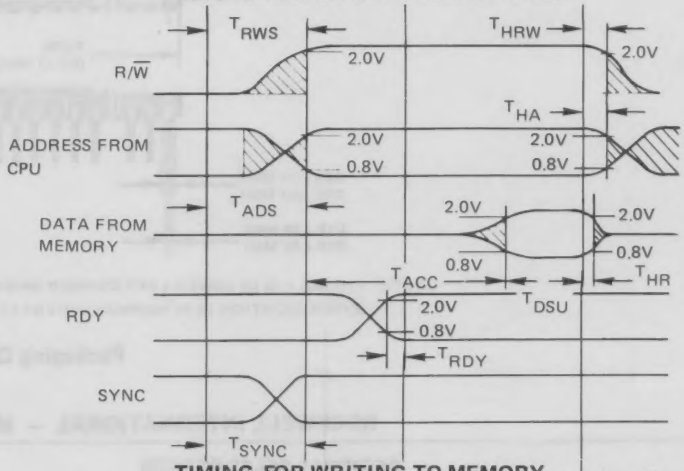
NOTES
(1) Additional 1024 bytes are decoded for external memory addressing by the R6500/1E Emulator Device. This area can be used during debug, but cannot be used in a masked ROM R6500/1.
(2) I/O command only; i.e., no stored data.
(3) Clears Counter Overflow — Bit 7 in Control Register
(4) CAUTION: The R6500/1E allows RAM mapping into 040-07F, 100-13F, 140-17F, 200-23F, 240-27F, 300-33F, and 340-37F; as well as 000-03F. The production R6500/1, however allows RAM mapping only at 000-03F.

R6500/1E TIMING DIAGRAMS

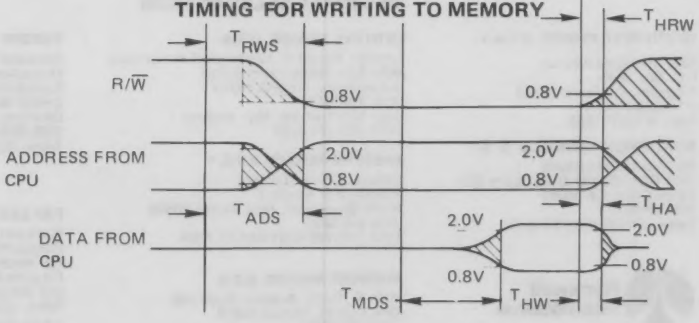
PHASE 2 (ϕ2) TIMING REFERENCE



TIMING FOR READING FROM MEMORY



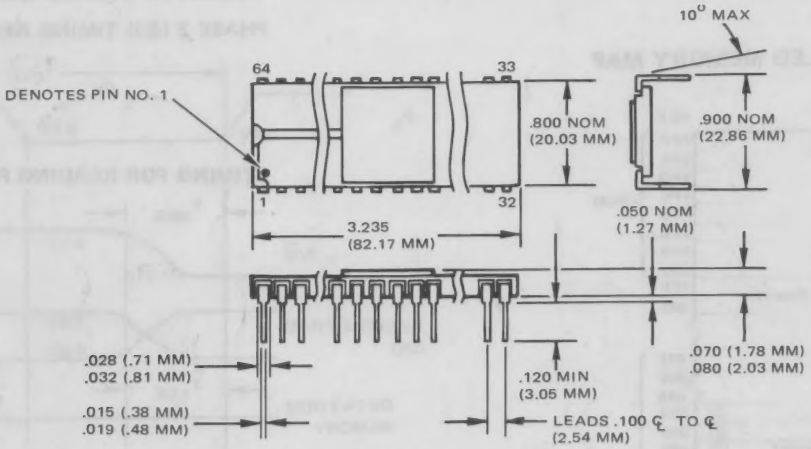
TIMING FOR WRITING TO MEMORY



ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 ± 5%, V_{SS} = 0, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Threshold Voltage D0-D7, RDY,	V_{IHT}	V_{SS} + 2.4	–	–	Vdc
Input Low Threshold Voltage D0-D7, RDY,	V_{ILT}	–	–	V_{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V = 0.4 to 2.4V, V_{CC} = 5.25V) D0-D7	I_{TSI}	–	–	10	μA
Output High Voltage (I_{LOAD} = 100μ Adc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, φ2	V_{OH}	V_{SS} + 2.4	–	-	Vdc
Output Low Voltage (I_{LOAD} = 1.6 mAdc, V_{CC} = 4.75V) D0-D7, SYNC, A0-A11, R/$\overline{W}$, φ2	V_{OL}	–	–	V_{SS} + 0.6	Vdc
Power Dissipation	P_D	–	0.75	1.20	W
Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz) RDY D0-D7 A0-A11, R/$\overline{W}$, SYNC φ2	C C_{in} C_{out} $C_{\phi 2}$	 – – – –	 – – – 50	 10 15 12 80	pF
I/O Port Pull-up Resistance	R_L	3.0	6.0	11.5	kohm



NOTE: PIN NO. 1 IS IN LOWER LEFT CORNER WHEN SYMBOLIZATION IS IN NORMAL ORIENTATION

Packaging Diagram

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R6500 Microcomputer System
PRODUCT PREVIEW

R6500/1-11Q ONE-CHIP MICROCOMPUTER

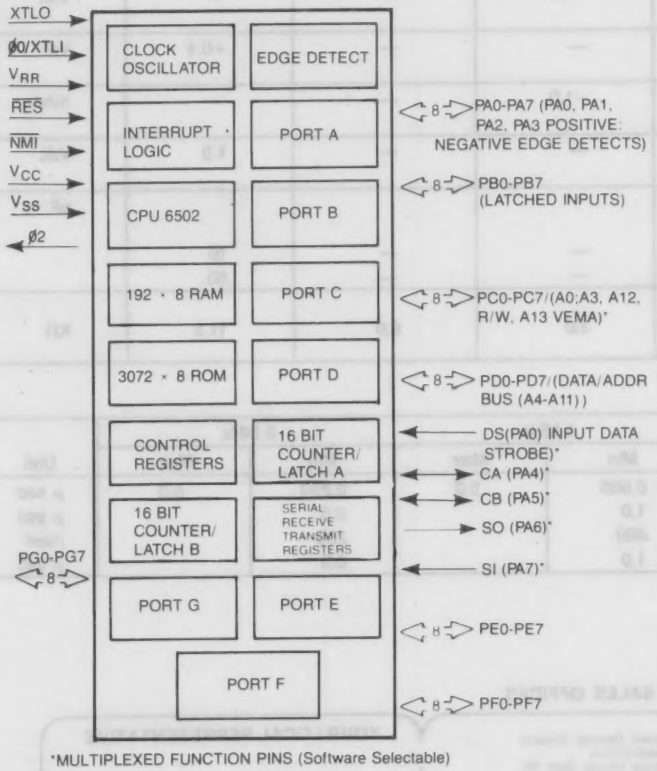
INTRODUCTION

The Rockwell R6500/1-11Q is a complete, high-performance 8-bit NMOS-3 microcomputer on a single chip, and is compatible with all members of the R6500 family.

The R6500/1-11Q consists of an enhanced 6502 CPU, an internal clock oscillator, 3072 bytes of Read-Only Memory, 192 bytes of Random Access Memory (RAM) and versatile interface circuitry. The interface circuitry includes two 16-bit programmable timer/counters, 56 bidirectional input/output lines (including four edge-sensitive lines and input latching on one 8-bit port), a full-duplex serial I/O channel, ten interrupts and bus expandability.

DEVELOPMENT SUPPORT

To allow prototype circuit development, Rockwell offers a PROM-compatible 64-pin Emulator device. This device, the R6500/2-11, provides all R6500/1-11Q interface lines (except Ports E, F and G), plus the address bus, data bus and control lines to interface with external memory. The R6500/2-11 may also be used as a CPU-RAM-I/O counter device in multichip systems.



*MULTIPLEXED FUNCTION PINS (Software Selectable)

Interface Diagram

Rockwell supports development of the R6500/1-11Q with the System 65 Microcomputer Development System and the R6500/1-11 Personality Module. Complete in-circuit emulation with the R6500/1-11Q Personality Module allows total system test and evaluation.

FEATURES

- Enhanced 6502 CPU
  - —Four new instructions
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 3K-byte mask-programmable ROM
- 192-byte static RAM
- 56 bidirectional, TTL-compatible I/O lines (seven ports)
- One 8-bit port may be tri-stated under software control
- One 8-bit port has Darlington drive capability
- One 8-bit port with programmable latched input
- Two 16-bit programmable counter/timers, with latches
  - —Pulse measurement
  - —Pulse generation
  - —Interval timer
  - —Event counter
- Serial port
  - —Full-duplex asynchronous operation mode
  - —Synchronous shift register mode
  - —Selectable 5- to 8-bit characters
  - —Wake-up feature
  - —Programmable bit rates to 62.5 bits/sec (@ 2 MHz)
- Four edge-sensitive lines; two positive, two negative
- Ten interrupts
  - —Reset
  - —Non-maskable
  - —Four external, edge-sensitive
  - —Two counter
  - —Serial data received
  - —Serial data transmitted
- Bus expandable to 16K bytes of external memory
- Flexible clock circuitry
  - —2-MHz or 1-MHz internal operation
  - —Internal clock with external XTAL at two or four times internal frequency
  - —External clock input divided by one, two or four
- 1 μs minimum instruction execution time
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 16 mW stand-by power for 32 bytes of the 192-byte RAM
- 64-pin QUIP

Specifications subject to change without notice
Document No. 29000 D65
Rev. 1, October 1980

ELECTRICAL SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{in}	−0.3 to +7.0	Vdc
Operating Temperature Range, Commercial Industrial	T	0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

D.C. Characteristics (V_{CC} = 5V ±5% V_{CC} = 0)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Dissipation (Outputs High) Commercial @ 25°C Industrial @ 25°C	P_D	— —		1000 1200	mW
RAM Standby Voltage (Retention Mode)	V_{RR}	3.0	—	V_{CC}	Vdc
RAM Standby Current (Retention Mode) Commercial @ 25°C Industrial @ 25°C	I_{RR}	— —	4 5.2	— —	mAdc
Input High Voltage (Except XTLI)	V_{IH}	+2.0	—	V_{CC}	Vdc
Input High Voltage (XTLI)	V_{IH}	+4.0	—	V_{CC}	Vdc
Input Low Voltage	V_{IL}	−0.3	—	+0.8	Vdc
Input Leakage Current (RES, NMI) V_{in} = 0 to 5.0 Vdc	I_{IN}		±1.0	±2.5	μAdc
Input Low Current PA, PB, PC, PD, PF, and PG (V_{IL} = 0.4 Vdc)	I_{IL}	—	−1.0	−1.6	mAdc
Output High Voltage Except XTLO (I_{Load} = .100 μAdc)	V_{OH}	+2.4	—	—	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc)	V_{OL}	—	—	+0.4	Vdc
Darlington Current Drive, PEO~PE7 (V_o = 1.5 Vdc)	I_{OH}	−1.0	—	—	mAdc
Output Low Voltage, PEO~PE7 (I_{Load} = 10 mAdc sink)	V_{OL}	—	—	1.0	Vdc
Input Capacitance (V_{in}-0, T_A = 25°C, f=1.0 MHz) PA, PB, PC, PD, PF, and PG XTLI, XTLO	C_{in}	— —	— —	10 50	pF
I/O Port Pull-Up Resistance PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7, PF0-PF7 & PG0-PG7	R_L	3.0	6.0	11.5	KΩ

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

AC Characteristics (V_{CC} = 5V ±5% V_{SS} = 0)

Parameter	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
XTLI Input Clock Cycle Time	T_{cyc}	0.500	5.0	0.250	5.0	μ sec
Internal Write to Peripheral Data Valid (TTL)	T_{PDW}	1.0		0.5		μ sec
Peripheral Data Setup Time	T_{PDSU}	400		200		nsec
Count and Edge Detect Pulse Width	T_{PW}	1.0		0.5		μ sec

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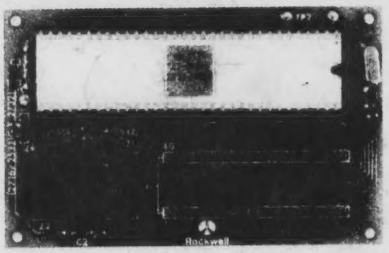
DOCUMENT NO. 29650 N59
REV. 1, MAY 1980

PART NUMBER
M65-089

Rockwell

R6500 Microcomputer System
PRODUCT DESCRIPTION

R6500/1 EVALUATION MODULE



INTRODUCTION

The R6500/1 Evaluation Module allows a computer program developed for R6500/1 Single Chip Microcomputer to be executed in a stand-alone manner using the R6500/1EAC Emulator Device and an associated PROM. With this capability, the computer program can be validated before being masked into the R6500/1 ROM.

The R6500/1 Evaluation Module consists of:

- An R6500/1 Emulator Board containing:
  - — One R6500/1EAC Emulator Device
  - — One 2-MHz crystal
  - — One 7404 Hex Inverter
  - — Seven jumper positions
  - — One 24-pin socket for a PROM
- A 40-conductor ribbon cable terminated at each end with a 40-pin connector

REFERENCE DOCUMENTS

R6500/1 One-Chip Microcomputer Data Sheet, 29000 D51
R6500/1E Emulator Device Data Supplement, 29000 D51S
R6500/1 One-Chip Microcomputer Product Description, 29650 N48

Document 29000 D51S describes operational differences between the R6500/1 Microcomputer and the R6500/1E Emulator Device.

INSTALLATION PROCEDURE

CAUTION

Ensure power is disconnected from the R6500/1 socket in the user circuit before connecting the R6500/1 Evaluation Module or damage may occur to the user circuit and/or the R6500/1 Evaluation Module.

1. Plug the PROM containing the R6500/1E program into socket Z2 while carefully observing the Pin 1 position. Any of the following PROMs (or compatible equivalents) may be used:

PROM	NO. OF BYTES	INSTALLED ADDRESS RANGE
Intel 2716	2K	$800-$FFF
TI TMS2516	2K	$800-$FFF
Intel 2732	4K	$400-$FFF*
TI TMS2532	4K	$400-$FFF*

*Addresses $400-$FFF may be used only with the R6500/1E and are not available in the R6500/1 ROM. Note that only the upper 3K bytes of a 4K-byte PROM may be used.

2. Install the jumpers as follows:

a. Jumpers D and E—Clock Select

Jumpers D and E select the desired crystal or clock configuration.

FREQUENCY REFERENCE	JUMPER D	JUMPER E
R6500/1 Emulator Module Crystal	OUT	OUT
User Circuit Crystal*	IN	IN
User Circuit Clock*	IN	OUT

*Disconnect Crystal Y1 from the R6500/1E Emulator Device by unsoldering the crystal leads from posts E1 and E2. Users who install a 4MHz crystal must use a PROM with an access time less than 225 ns.

b. Jumpers A, B, C, F, and G—PROM Select

Jumpers A, B, C, F and G configure the Emulator Module to operate with the desired PROM.

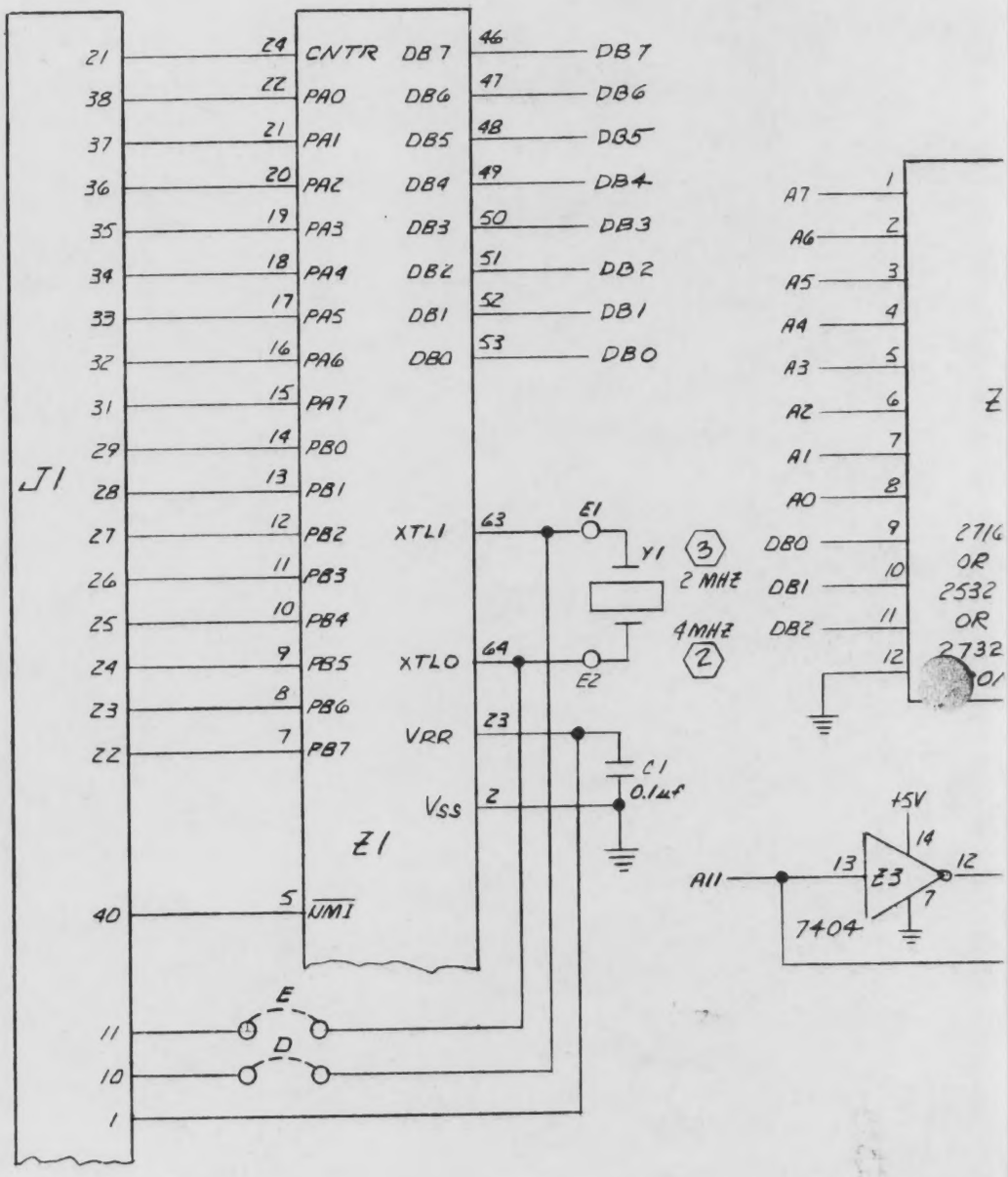
PROM	JUMPERS A	B	C	F	G
2516	IN	OUT	OUT	OUT	IN
2716	IN	OUT	OUT	OUT	IN
2532	OUT	IN	OUT	OUT	IN
2732	OUT	OUT	IN	IN	OUT

3. Connect the R6500/1 Emulator Module to the user circuit in either of two ways:

   a. Connect P1 of the interface cable into J1 of the R6500/1 Emulator Module and J1 of the interface cable into the R6500/1 socket in the user circuit.

   b. Directly connect the extended pins of J1 on the R6500/1 Emulator Module into the R6500/1 socket in the user circuit.

4. Apply power to the user circuit.



NOTE: UNLESS OTHERWISE SPECIFIED

1. REFERENCE ASSEMBLY DRAWING PS01-D100

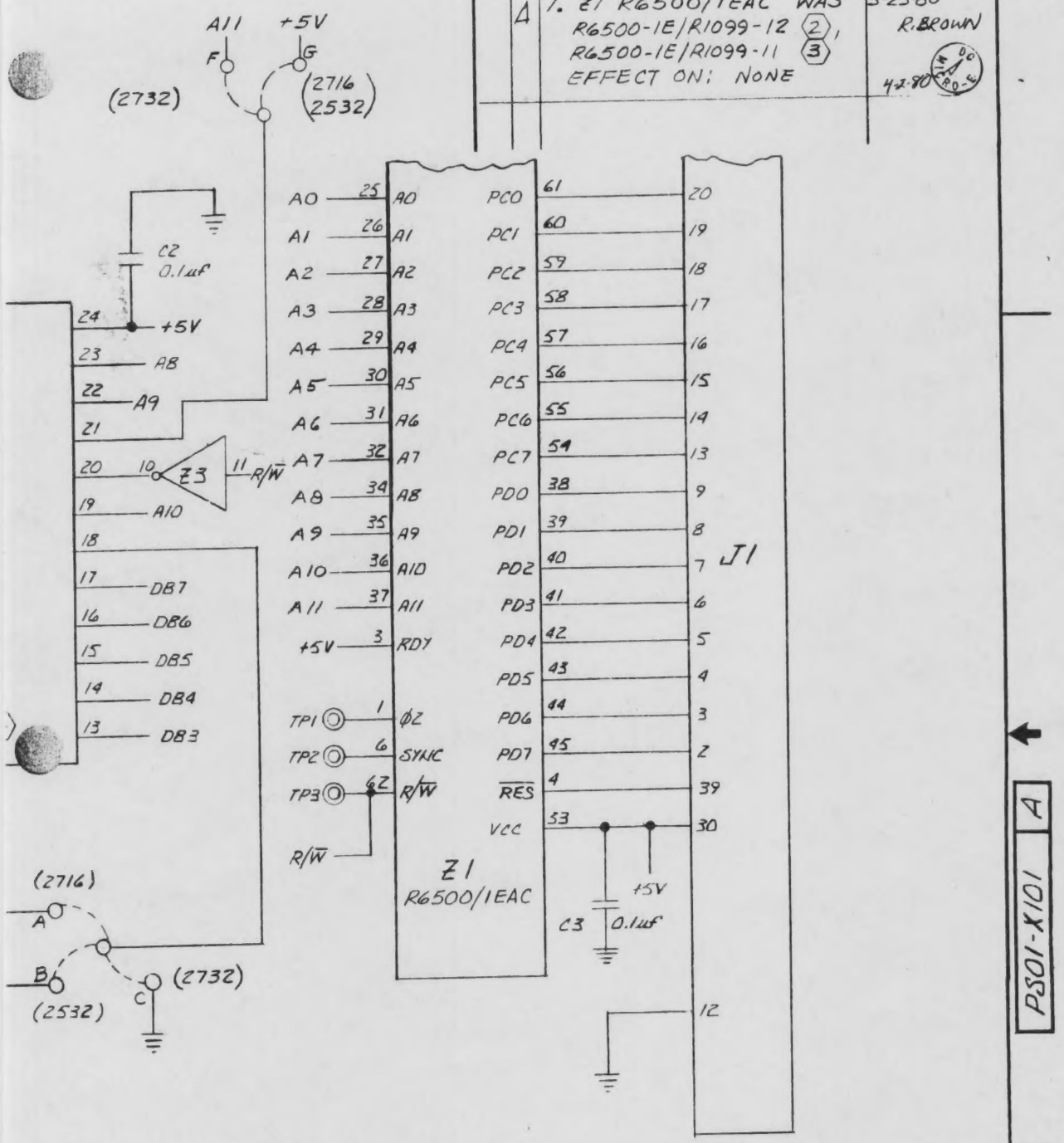
(2) USED ON -001 ASSY

(3) USED ON -011 ASSY

(4) -001 ASSEMBLY REQUIRES A PROM DEVICE WITH ACCESS TIME LESS THAN 225 ns

A NC 7-25-79

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	1. Z1 R6500/1EAC WAS R6500-1E/R1099-12 (2), R6500-1E/R1099-11 (3) EFFECT ON: NONE	3-25-80	R. BROWN 4-2-80



PS01-X101 A

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX = ± .03 .XXX = ± .010 ANGLES ± 30'	AUTHORIZATION NO.	
MATERIAL:	DR BY	~~TREED~~ 4-2-79
HEAT TREAT	CHK BY	D. Eyman 7-12-79
FINISH	APPD BY	J. Miller 7/12/79
	APPD BY	

PART NO.

ROCKWELL INTERNATIONAL CORPORATION
MICROELECTRONIC DEVICES
3310 MIRALOMA AVE., ANAHEIM, CA 92803

SCHEMATIC DIAGRAM-
R6500/1 EVALUATION
MODULE

SIZE	CODE IDENT NO.	DRAWING NO.
C	34576	PS01-X101

SCALE NONE REV A SHEET

NO.	NEXT ASSY	USED ON

JUMPER DESCRIPTION

JUMPER A — Connects address line A11 to pin 18 of the PROM after inverting for 2716 operation.

JUMPER B — Connects address line A11 directly to pin 18 of the PROM for 2532 operation.

JUMPER C — Connects GND to pin 18 of the PROM for 2732 operation.

JUMPER D — Connects the high side of the external clock or crystal to pin 63 (XTLI) of the R6500/1E Emulator Device.

JUMPER E — Connects the low side of the external clock or crystal to pin 64 (XTLO) of the R6500/1E Emulator Device.

JUMPER F — Connects address line A11 to pin 21 of the PROM for 2732 operation.

JUMPER G — Connects +5V to pin 21 of the PROM for 2716 or 2532 operation.

PROM SOCKET INTERFACE SIGNALS

PROM Socket Pin Number	PROM Device Type			
	TI TMS2532	INTEL 2732	TI TMS2516	INTEL 2716
1	A7	A7	A7	A7
2	A6	A6	A6	A6
3	A5	A5	A5	A5
4	A4	A4	A4	A4
5	A3	A3	A3	A3
6	A2	A2	A2	A2
7	A1	A1	A1	A1
8	A0	A0	A0	A0
9	Q1	O0	Q1	O0
10	Q2	O1	Q2	O1
11	Q3	O2	Q3	O2
12	VSS	GND	VSS	GND
13	Q4	O3	Q4	O3
14	Q5	O4	Q5	O4
15	Q6	O5	Q6	O5
16	Q7	O6	Q7	O6
17	Q8	O7	Q8	O7
18	A11	$\overline{CE}$	PD/PGM	$\overline{CE}$/PGM
19	A10	A10	A10	A10
20	PD/$\overline{PGM}$	$\overline{OE}$/VPP	$\overline{CS}$	$\overline{OE}$
21	VPP	A11	VPP	VPP
22	A9	A9	A9	A9
23	A8	A8	A8	A8
24	VCC	VCC	VCC	VCC

COMPONENT DESCRIPTION

Connector J1 — Connector with extended pins that allows the R6500/1 Evaluation Module to be directly plugged into the R6500/1 connector in the user circuit or to be connected to the user circuit R6500/1 connector through the 40 conductor interface cable assembly.

Socket Z1 — 64-pin DIP socket that contains the R6500/1 EAC 2-MHz Emulator Device.

Socket Z2 — 24-pin DIP socket, which accepts the user-supplied program PROM

Crystal Y1 — A 2-MHz crystal, which is used to operate the R6500/1EAC Emulator Device at 1 MHz.

Inverter Z3 — Inverts R/$\overline{W}$ to provide a low on pin 20 of the PROM when R/W is high.

— Inverts A11 when jumper A is installed to provide a low on pin 18 ($\overline{CS}$) when 2716 is used.

Capacitors C1, C2, and C3—Bypass Capacitors.

Test Point TP1—Test point to monitor Ø2.

Test Point TP2—Test point to monitor SYNC.

Test Point TP3—Test point to monitor R/$\overline{W}$.

Post E1—Crystal solder post to XTLI.

Post E2—Crystal solder post to XTLO.

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YOUR LOCAL REPRESENTATIVE

DOCUMENT NO. 29000 D60
FEBRUARY, 1980

188.000

PART NUMBER
R6500/1EB

Rockwell

R6500 Microcomputer System DATA SHEET

R6500/1EB BACKPACK EMULATOR

INTRODUCTION

The Rockwell R6500/1EB Backpack Emulator is the PROM prototyping version of the 8-bit, masked-ROM R6500/1 one-chip microcomputer. Like the R6500/1, the R6500/1EB is totally upward/downward compatible with all members of the R6500 family. The R6500/1EB is designed to accept standard 5-volt, 24-pin PROMs, EPROMs or ROMs directly, in a socket on top of the Emulator. This packaging concept allows a standard EPROM to be easily removed, re-programmed, then reinserted as often as desired.

The R6500/1EB has the same pinouts as the masked-ROM R6500/1 microcomputer. These 40 pins are functionally and operationally identical to the pins on the R6500/1, with some minor differences (described herein). The R6500/1 Microcomputer Data Sheet (Rockwell Document No. 29000D51) includes a description of the interface signals and their functions. Whereas the masked-ROM R6500/1 provides 2K bytes of read-only memory, the R6500/1EB will address 3K bytes of external program memory. This extra memory accommodates program patches, test programs or optional programs during breadboard and prototype development states.

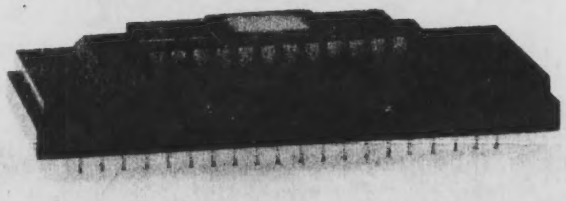
ORDERING INFORMATION

ORDER NUMBER	MEMORY CAPACITY	COMPATIBLE MEMORIES	TEMPERATURE RANGE
R6500/1EB-1	2K	2716,2516, 82S2708, 2316B	$0^{o}C$ to $70^{o}C$
R6500/1EB-2	3K	2532,2332, 82S2708	$0^{o}C$ to $70^{o}C$
R6500/1EB-3	3K	2732, 82S2708	$0^{o}C$ to $70^{o}C$
R6500/1EB-4	1K	2758, 82S2708	$0^{o}C$ to $70^{o}C$

PRODUCT SUPPORT

The R6500/1EB Backpack Emulator is just one of the products that Rockwell offers to facilitate system and program development for the R6500/1. Additional support products include the R6500/1E, a 64-pin emulator device with interface lines for connecting external memory. Another support product is the R6500/1 Evaluation Module, which has 40 R6500/1-compatible pins and provision for inserting external memory.

Further, the SYSTEM 65 Microcomputer Development System with R6500/1 Personality Module supports both hardware and software development. Complete in-circuit user emulation with the R6500/1 Personality Module allows total system test and evaluation. With the optional PROM Programmer, SYSTEM 65 can also be used to program EPROMs for the development activity. When PROM programs have been finalized, the PROM device can be sent to Rockwell for masking into the 2K ROM of the R6500/1. In addition to support products, Rockwell offers regularly-secheduled designers courses at regional centers.



The available support products include:

- SYSTEM 65 Microcomputer Development System — P/N S65-101
- PROM Programmer Module — P/N M65-040
- 1-MHz R6500/1 Personality Module — P/N M65-081
- 2-MHz R6500/1 Personality Module — P/N M65-082
- 1-MHz R6500/1 Emulator Device — P/N R6500/1EC
- 2-MHz R6500/1 Emulator Device — P/N R6500/1EAC
- R6500/1 Evaluation Module — P/N M65-089

FEATURES

- PROM version of the R6500/1
- Completely pin compatible with R6500/1 single-chip microcomputers
- Profile approaches 40 pin DIP of R6500/1
- Accepts 5 volt, 24 pin industry-standard EPROMs, PROMs, ROMs
  - 4K memories — 2532, 2732, 2332 (3K bytes addressable)
  - 2K memories — 2716, 2516, 2316B
  - 1K memories — 2758, 82S2708
- Use as prototyping tool or for low volume production
- 3K bytes of memory capacity (1K, 2K, 4K memories)
- 64 x 8 static RAM
- Separate power pin for RAM
- Software compatibility with the R6500 family
- 32 bi-directional TTL compatible I/O lines (4 ports)
- 1 bi-directional TTL compatible counter I/O line
- 16 bit programmable counter/latch with four modes (interval timer, pulse generator, event counter, pulse width measurement)
- 5 interrupts (reset, non-maskable, two external edge sensitive, counter)
- Crystal or extenal time base
- Single +5V power supply